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1 Compiler techniques for code compaction

Saumya K. Debray, William Evans, Robert Muth, Bjorn De Sutter

March 2000 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 22 Issue 2

Full text available: pdf(409.20 KB) Additional Information: full citation, abstract, references, citings, index terms, review

In recent years there has been an increasing trend toward the incorpor ation of computers into a variety of devices where the amount of memory available is limited. This makes it desirable to try to reduce the size of applications where possible. This article explores the use of compiler techniques to accomplish code compaction to yield smaller executables. The main contribution of this article is to show that careful, aggressive, interprocedural optimization, together with procedural abstr ...

Keywords: code compaction, code compression, code size reduction

2 Combining Global Code and Data Compaction

Bjorn De Sutter, Bruno De Bus, Koen De Bosschere, Saumya Debray

August 2001 **ACM SIGPLAN Notices**, Volume 36 Issue 8

Full text available: pdf(191.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Computers are increasingly being incorporated in devices with a limited amount of available memory. As a result research is increasingly focusing on the automated reduction of program size. Existing literature focuses on either data or code compaction or on highly language dependent techniques. This paper shows how combined code and data compaction can be achieved using a link-time code compaction system that reasons about the use of both code and data addresses. The analyses proposed rely on ...

3 Survey of code-size reduction methods

Árpád Beszédes, Rudolf Ferenc, Tibor Gyimóthy, André Dolenc, Konsta Karsisto

September 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 3

Full text available: pdf(443.89 KB) Additional Information: full citation, abstract, references, index terms

Program code compression is an emerging research activity that is having an impact in several production areas such as networking and embedded systems. This is because the reduced-sized code can have a positive impact on network traffic and embedded system costs such as memory requirements and power consumption. Although code-size reduction is a relatively new research area, numerous publications already exist on it. The methods published usually have different motivations and a variety of appli ...

Keywords: code compaction, code compression, method assessment, method evaluation

4 Time-constrained code compaction for DSPs

Rainer Leupers, Peter Marwedel

September 1995 **Proceedings of the 8th international symposium on System synthesis**

Full text available: pdf(175.99 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Abstract: DSP algorithms are, in most cases, subject to hard real-time constraints. In the case of programmable DSPs, meeting those constraints must be ensured by appropriate code generation techniques. For processors offering instruction-level parallelism, the task of code generation includes code compaction. The exact timing behavior of a DSP program is only known after compaction. Therefore, real-time constraints should be taken into account during the compaction phase. While most known DSP c ...

Keywords: automatic programming, code generation techniques, digital signal processing algorithms, digital signal processing chips, encoding restrictions, exact timing behavior, hard real-time constraints, instruction-level parallelism, integer programming, integer programming model, local code compaction, programmable DSP, real-time systems, rigid heuristics, side-effects, source coding, time-constrained code compaction, timing

5 Sifting out the mud: low level C++ code reuse
Bjorn De Sutter, Bruno De Bus, Koen De Bosschere
November 2002 **ACM SIGPLAN Notices , Proceedings of the 17th ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications,** Volume 37 Issue 11
Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, citings, index terms

More and more computers are being incorporated in devices where the available amount of memory is limited. This contrasts with the increasing need for additional functionality and the need for rapid application development. While object-oriented programming languages, providing mechanisms such as inheritance and templates, allow fast development of complex applications, they have a detrimental effect on program size. This paper introduces new techniques to reuse the code of whole procedures at t ...

Keywords: code compaction, code size reduction

6 Prophetic branches: a branch architecture for code compaction and efficient execution
Apoorv Srivastava, Alvin M. Despain
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**
Full text available: pdf(571.93 KB) Additional Information: full citation, references, citings

7 Software techniques for program compaction: Post-pass compaction techniques
Bruno De Bus, Daniel Kästner, Dominique Chanet, Ludo Van Put, Bjorn De Sutter
August 2003 **Communications of the ACM,** Volume 46 Issue 8
Full text available: pdf(120.98 KB) html (34.37 KB) Additional Information: full citation, abstract, references, citings, index terms

Seeking to resolve many of the problems related to code size in traditional program development environments.

8 Code size reduction technique and implementation for software-pipelined DSP applications
Qingfeng Zhuge, Bin Xiao, Edwin H.-M. Sha
November 2003 **ACM Transactions on Embedded Computing Systems (TECS),** Volume 2 Issue 4
Full text available: pdf(371.88 KB) Additional Information: full citation, abstract, references, citings, index terms

Software pipelining technique is extensively used to exploit instruction-level parallelism of loops, but also significantly expands the code size. For embedded systems with very limited on-chip memory resources, code size becomes one of the most important optimization concerns. This paper presents the theoretical foundation of code size reduction for software-pipelined loops based on retiming concept. We propose a general Code-size REDuction technique (CRED) for various kinds of processors. Our ...

Keywords: DSP processors, Retiming, scheduling, software pipelining

9 Generation of fast interpreters for Huffman compressed bytecode
Mario Latendresse, Marc Feeley
June 2003 **Proceedings of the 2003 workshop on Interpreters, virtual machines and emulators**
Full text available: pdf(323.22 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems often have severe memory constraints requiring careful encoding of programs. For example, smart cards have on the order of 1K of RAM, 16K of non-volatile memory, and 24K of ROM. A virtual machine can be an effective approach to obtain compact programs but instructions are commonly encoded using one byte for the opcode and multiple bytes for the operands, which can be wasteful and thus limit the size of programs runnable on embedded systems. Our approach uses canonical Huffman co ...

Keywords: Java, canonical Huffman code, code compression, decoder

10 Extending microcode compaction for real architectures
Mark Harris
December 1987 **Proceedings of the 20th annual workshop on Microprogramming**
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings

Microcode compaction is an essential component of any high-level language compiler that generates microcode for a horizontal architecture machine. Recent research into both local and global compaction has assumed the use of a simple abstract machine. Although this assumption simplifies the effort considerably, it neglects addressing and timing problems brought on by the uncommon operation of some machines. This paper discusses both local and global compaction in ...

11 Software techniques for program compaction: Introduction
Bjorn De Sutter, Koen De Bosschere
August 2003 **Communications of the ACM**, Volume 46 Issue 8
Full text available: pdf(61.26 KB) html (11.47 KB) Additional Information: full citation, references, index terms

12 Timestamped whole program path representation and its applications
Youtao Zhang, Rajiv Gupta
May 2001 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2001 conference on Programming language design and implementation**, Volume 36 Issue 5
Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

A *whole program path* (WPP) is a complete control flow trace of a program's execution. Recently Larus [18] showed that although WPP is expected to be very large (100's of MBytes), it can be greatly compressed (to 10's of MBytes) and therefore saved for future analysis. While the compression algorithm proposed by Larus is highly effective, the compression is accompanied with a loss in the ease with which subsets of information can be accessed. In particular, path traces pertaining to a p ...

13 Local Microcode Compaction Techniques
David Landskov, Scott Davidson, Bruce Shriver, Patrick W. Mallett
September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3
Full text available: pdf(2.83 MB) Additional Information: full citation, references, citings, index terms

14 Code generation schema for modulo scheduled loops
B. Ramakrishna Rau, Michael S. Schlansker, P. P. Tirumalai
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2
Full text available: pdf(1.49 MB) Additional Information: full citation, references, citings, index terms

15 Instruction selection for embedded DSPs with complex instructions
R. Leupers, P. Marwedel
September 1996 **Proceedings of the conference on European design automation**
Full text available: pdf(290.83 KB) Additional Information: full citation, references, citings, index terms

16 A dynamic-programming technique for compacting loops
Stephen R. Vegdahl
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2
Full text available: pdf(1.27 MB) Additional Information: full citation, references, citings, index terms

Keywords: compaction, dynamic programming, horizontal, pipelining, scheduling

17 A development environment for horizontal microcode programs
A. Aiken, A. Nicolau
December 1986 **ACM SIGMICRO Newsletter , Proceedings of the 19th annual workshop on Microprogramming**, Volume 17 Issue 4
Full text available: pdf(949.10 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a development environment for horizontal microcode. The environment uses Percolation Scheduling, a transformational system for parallelism extraction, and an interactive profiling system to give the user control over the microcode compaction process while reducing the burdensome details of architecture, correctness preservation, and synchronization. Through a graphical interface the user suggests what should be done in parallel, while the system performs the actual chan ...

18 Issues of the design of a low level microprogramming language for global microcode compaction
Michael D. Poe, Ross Goodell, Simon Steely
December 1981 **ACM SIGMICRO Newsletter , Proceedings of the 14th annual workshop on Microprogramming**, Volume 12 Issue 4
Full text available: pdf(599.91 KB) Additional Information: full citation, abstract, references, citings, index terms

Microcode compaction, or packing, is the process of assigning microoperations to microwords so that the minimum number of microwords and execution time is used by the microprogram. The techniques for global microcode compaction have been described elsewhere (see below). This paper describes a proposal for an intermediate level language approach to compilation which allows machine independent global compaction. We will call the program which does this compaction the packer. This work comes f ...

19 A Dynamic Programming Approach to Optimal Integrated Code Generation
Christoph Keßler, Andrzej Bednarski
August 2001 **ACM SIGPLAN Notices**, Volume 36 Issue 8
Full text available: pdf(216.58 KB) Additional Information: full citation, abstract, references, citings, index terms

Phase-decoupled methods for code generation are the state of the art in compilers for standard processors but generally produce code of poor quality for irregular target architectures such as many DSPs. In that case, the generation of efficient code requires the simultaneous solution of the main subproblems instruction selection, instruction scheduling, and register allocation, as an integrated optimization problem.

In contrast to compilers for standard processors, code generation for ...

Keywords: dynamic programming, instruction scheduling, instruction selection, integrated code generation, register allocation, time profile

20 Efficient handling of multiple inheritance hierarchies
Yves Caseau
October 1993 **ACM SIGPLAN Notices , Proceedings of the eighth annual conference on**

Object-oriented programming systems, languages, and applications, Volume 28 Issue 10
Full text available: pdf(1.63 MB) Additional Information: full citation, references, citings, index terms

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1 Adaptive link layer strategies for energy efficient wireless networking
Paul Lettieri, Curt Schurgers, Mani Srivastava
October 1999 **Wireless Networks**, Volume 5 Issue 5
Full text available: pdf(611.81 KB) Additional Information: full citation, references, citings, index terms

2 Data cache sizing for embedded processor applications
P. R. Panda, N. D. Dutt, A. Nicolau
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(38.44 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present a technique for determining the best data cache size required for a given memory-intensive application. A careful memory and cache line assignment strategy based on the analysis of the array access patterns effects a significant reduction in the required data cache size, with no negative impact on the performance, thereby freeing vital on-chip silicon area for other hardware resources. Experiments on several benchmark kernels performed on LSI Logic's CW4001 embedded processor simulato ...

3 Optimization: Transistor sizing of energy-delay–efficient circuits
Paul I. Pénzes, Mika Nyström, Alain J. Martin
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**
Full text available: pdf(207.24 KB) Additional Information: full citation, abstract, references, index terms

This paper studies the problem of transistor sizing of CMOS circuits optimized for energy-delay efficiency, i.e., for optimal Et^n where E is the energy consumption and t is the delay of the circuit, while n is a fixed positive optimization index that reflects the chosen trade-off between energy and delay.We propose a set of analytical formulas that closely approximate the optimal transistor sizes. We then study an efficient iteration procedure that can furt ...

Keywords: energy-delay optimization, transistor sizing

4 A case for source-level transformations in MATLAB
Vijay Menon, Keshav Pingali
December 1999 **ACM SIGPLAN Notices , Proceedings of the 2nd conference on Domain-specific languages**, Volume 35 Issue 1
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we discuss various performance overheads in MATLAB codes and propose different program transformation strategies to overcome them. In particular, we demonstrate that high-level source-to-source transformations of MATLAB programs are effective in obtaining substantial performance gains regardless of whether programs are interpreted or later compiled into C or FORTRAN. We argue that automating such transformations provides a promising area of future research.

5 Human-computer interface development: concepts and systems for its management
H. Rex Hartson, Deborah Hix
March 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 1
Full text available: pdf(7.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Human-computer interface management, from a computer science viewpoint, focuses on the process of developing quality human-computer interfaces, including their representation, design, implementation, execution, evaluation, and maintenance. This survey presents important concepts of interface management: dialogue independence, structural modeling, representation, interactive tools, rapid prototyping, development methodologies, and control structures. *Dialogue independence* is th ...

6 Implementation techniques: Exploring the barrier to entry: incremental generational garbage collection for Haskell
A. M. Cheadle, A. J. Field, S. Marlow, S. L. Peyton Jones, R. L. While
October 2004 **Proceedings of the 4th international symposium on Memory management**
Full text available: pdf(458.55 KB) Additional Information: full citation, abstract, references, index terms

We document the desi n and implementation of a "production" incremental garbage collector for GHC 6.2.It builds on our earlier work (Non-stop Haskell)that exploited GHC's dynamic dispatch mechanism to hijack object code pointers so that objects in to-space automatically scavenge themselves when the mutator attempts to "enter" them. This paper details various optimisations based on code specialisation that remove the dynamic space,and associated time, overheads that accompanied our earlier sch ...

Keywords: incremental garbage collection, non-stop haskell

7 Speeding up an overrelaxation method of division in Radix-2n machine
Hitohisa Asai, C. K. Cheng
March 1983 **Communications of the ACM**, Volume 26 Issue 3
Full text available: pdf(495.52 KB) Additional Information: full citation, abstract, references, index terms

For normalized floating point division, digital computers can take advantage of a division process that uses an iterative multiplying operation instead of repeated subtractions. An improvement of this division process by using accelerating constants in the overrelaxation has previously been proposed. Multiplication by a chosen accelerating constant accelerates the process of generating accurate digits of a quotient in division. We propose a further improvement by generalizing the ac ...

Keywords: Wilkes-Harvard scheme, algebraic algorithms, convergence, convergence division, iterative multiplication, overrelaxation, power series, truncation error

8 Task scheduling and real-time: Task-level timing models for guaranteed performance in multiprocessor networks-on-chip
P. Poplavko, T. Basten, M. Bekooij, J. van Meerbergen, B. Mesman
October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**
Full text available: pdf(299.73 KB) Additional Information: full citation, abstract, references, index terms

We consider a dynamic application running on a multiprocessor network-on-chip as a set of independent jobs, each job possibly running on multiple processors. To provide guaranteed quality and performance, the scheduling of jobs, jobs themselves and the hardware must be amenable to *timing analysis*. For a certain class of applications and multiprocessor architectures, we propose *exact timing models* that effectively co-model both the computation and communication of a job. The models ...

Keywords: buffer minimization, data flow graph, network-on-chip, performance evaluation, real-time, system-on-chip

9 Library-less synthesis for static CMOS combinational logic circuits

S. Gavrilov, A. Glebov, S. Pullela, S. C. Moore, A. Dharchoudhury, R. Panda, G. Vijayan, D. T. Blaauw
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(98.66 KB) Publisher Site	Additional Information: full citation, abstract, references, citings, index terms

Traditional synthesis techniques optimize CMOS circuits in two phases: i) logic minimization and ii) library mapping phase. Typically, the structures and the sizes of the gates in the library are chosen to yield good synthesis results over many blocks or even for an entire chip. Consequently this approach precludes an optimal design of individual blocks which may need custom structures. The authors present a new transistor level technique that optimizes CMOS circuits both structurally and size-w ...

Keywords: CMOS logic circuits, circuit performance, design space, library-less synthesis, optimal design, resynthesized circuits, size-wise CMOS circuit optimization, static CMOS combinational logic circuits, structural CMOS circuit optimization, transistor level technique

10 CAD: A high level language for pre-layout extraction in parasite-aware analog circuit synthesis
Raoul F. Badaoui, Hemanth Sampath, Anuradha Agarwal, Ranga Vemuri
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(1.47 MB)	Additional Information: full citation, abstract, references, index terms

This paper presents a high-level language MSL, for the specification of parameterized, topology-specific circuit extractors. Upon compilation, the MSL program yields an executable module which generates the extracted circuit containing parasitics, passive and active devices when given specific sizes. In contrast to traditional post-layout extraction, this is done *without* ever generating a layout. We call this *pre-layout extraction*. Pre-layout extraction is much faster than post-lay ...

Keywords: MSL, analog VLSI, parasitics, pre-layout extraction

11 Article abstracts with full text online: Reengineering of database intensive application
Rakesh Agarwal, Ajit Sarangi, Swati Das
May 2003 **ACM SIGSOFT Software Engineering Notes**, Volume 28 Issue 3

Full text available: pdf(223.18 KB)	Additional Information: full citation, abstract, references

Reengineering databases has been a challenge since ages and it requires process mapping to understand better and significantly improve the business processes and performance. In this paper we describe a generic architecture for reengineering legacy databases, which is an outcome of working on a real software project. The goal of this research is to formalize a process that is applicable to different database reengineering scenarios and requirements. We elaborate the steps that were actually done ...

Keywords: application development, database, legacy system, reengineering

12 Device-level early floorplanning algorithms for RF circuits
Mehmet Aktuna, Rob A. Rutenbar, L. Richard Carley
April 1998 **Proceedings of the 1998 international symposium on Physical design**

Full text available: pdf(1.14 MB)	Additional Information: full citation, abstract, references, citings, index terms

High-frequency circuits are notoriously difficult to lay out because of the tight coupling between device-level placement and wiring. Given that successful electrical performance requires careful control of the lowest-level geometric features—wire bends, precise length, proximity, planarity, etc.—we suggest a new layout strategy for these circuits: early floorplanning at the device level. This paper develops a floorplanner for RF circuits based on a genetic algorithm (GA) that s ...

13 Memory system characterization of commercial workloads
Luiz André Barroso, Kourosh Gharachorloo, Edouard Bugnion
April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.68 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Commercial applications such as databases and Web servers constitute the largest and fastest-growing segment of the market for multiprocessor servers. Ongoing innovations in disk subsystems, along with the ever increasing gap between processor and memory speeds, have elevated memory system design as the critical performance factor for such workloads. However, most current server designs have been optimized to perform well on scientific and engineering workloads, potentially leading to design dec ...

14 GKS/Ada post mortem, a cost analysis
Sam Harbaugh, Greg Saunders
December 1987 **Proceedings of the 1987 annual ACM SIGAda international conference on Ada**
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, index terms

This paper presents results and conclusions of a Research Program which, among other tasks, performed analyses of empirical data gathered from completed Ada projects and explored alternative methods for Ada cost modeling and estimation. Among others, the project performed a detailed parametric cost analysis on a 140,000 line of code implementation of the ANSI/ISO standard Graphical Kernel System (GKS). [1]. This paper presents detailed data and the results of comparing the semico ...

15 A trace-based evaluation of adaptive error correction for a wireless local area network
David A. Eckhardt, Peter Steenkiste
December 1999 **Mobile Networks and Applications**, Volume 4 Issue 4
Full text available: pdf(243.29 KB) Additional Information: full citation, abstract, references, citings, index terms

Wireless transmissions are highly susceptible to noise and interference. As a result, the error characteristics of a wireless link may vary widely depending on environmental factors such as location of the communicating systems and activity of competing radiation sources, making error control a difficult task. In this paper we evaluate error control strategies for a wireless LAN. Based on low-level packet traces of WaveLAN, we first show that forward error correction (FEC) is effective in r ...

16 Power, buffering and open source: An efficient surface-based low-power buffer insertion algorithm
Rajeev R. Rao, David Blaauw, Dennis Sylvester, Charles J. Alpert, Sani Nassif
April 2005 **Proceedings of the 2005 international symposium on physical design**
Full text available: pdf(512.45 KB) Additional Information: full citation, abstract, references, index terms

Buffer insertion is an important technique used to achieve timing closure in high performance VLSI designs. As the number of buffers in ASIC designs has increased with process scaling, the power con-sumption of buffers has become a critical concern. In this paper, we present an efficient algorithm that performs van Ginneken style buffer insertion on RC trees and minimizes the total power con-sumption under a given delay constraint. Our algorithm is based on a formulation that uses a buffer libra ...

Keywords: buffer insertion, low-power design, physical synthesis

17 Algorithm 573: NL2SOL—An Adaptive Nonlinear Least-Squares Algorithm [E4]
John E. Dennis, David M. Gay, Roy E. Welsch
September 1981 **ACM Transactions on Mathematical Software (TOMS)**, Volume 7 Issue 3
Full text available: pdf(909.92 KB) Additional Information: full citation, references, citings, index terms

18 Session 5: Fine-grain CAM-tag cache resizing using miss tags
Michael Zhang, Krste Asanović
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**
Full text available: pdf(220.91 KB) Additional Information: full citation, abstract, references, citings, index terms.

A new dynamic cache resizing scheme for low-power CAM-tag caches is introduced. A control algorithm that is only activated on cache misses uses a duplicate set of tags, the **miss tags**, to minimize active cache size while sustaining close to the same hit rate as a full size cache. The cache partitioning mechanism saves both switching and leakage energy in unused partitions with little impact on cycle time. Simulation results show that the scheme saves 28--56% of data cache energy and 34--49 ...

Keywords: cache resizing, content-addressable-memory, energy efficiency, leakage current, low-power

19 Ada simulation technology - methods and metrics
John E. Melde, Philip G. Gage
January 1988 **Proceedings of the 21st annual symposium on Simulation**
Full text available: pdf(1.53 MB) Additional Information: full citation, abstract, references, index terms

This paper describes the impact of the Ada programming language on the development and use of simulation models. Based upon the development in Ada of a discrete-event simulation package (A*SIM), Ada is shown to provide numerous language features and methodologies that are ideally suited for modeling and simulation. Productivity and performance metrics collected during development and extensive use of A*SIM are also presented to provide quantitative comparisons of Ada-based modeling and simu ...

20 Analog circuit sizing based on formal methods using affine arithmetic
Andreas Lemke, Lars Hedrich, Erich Barke
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
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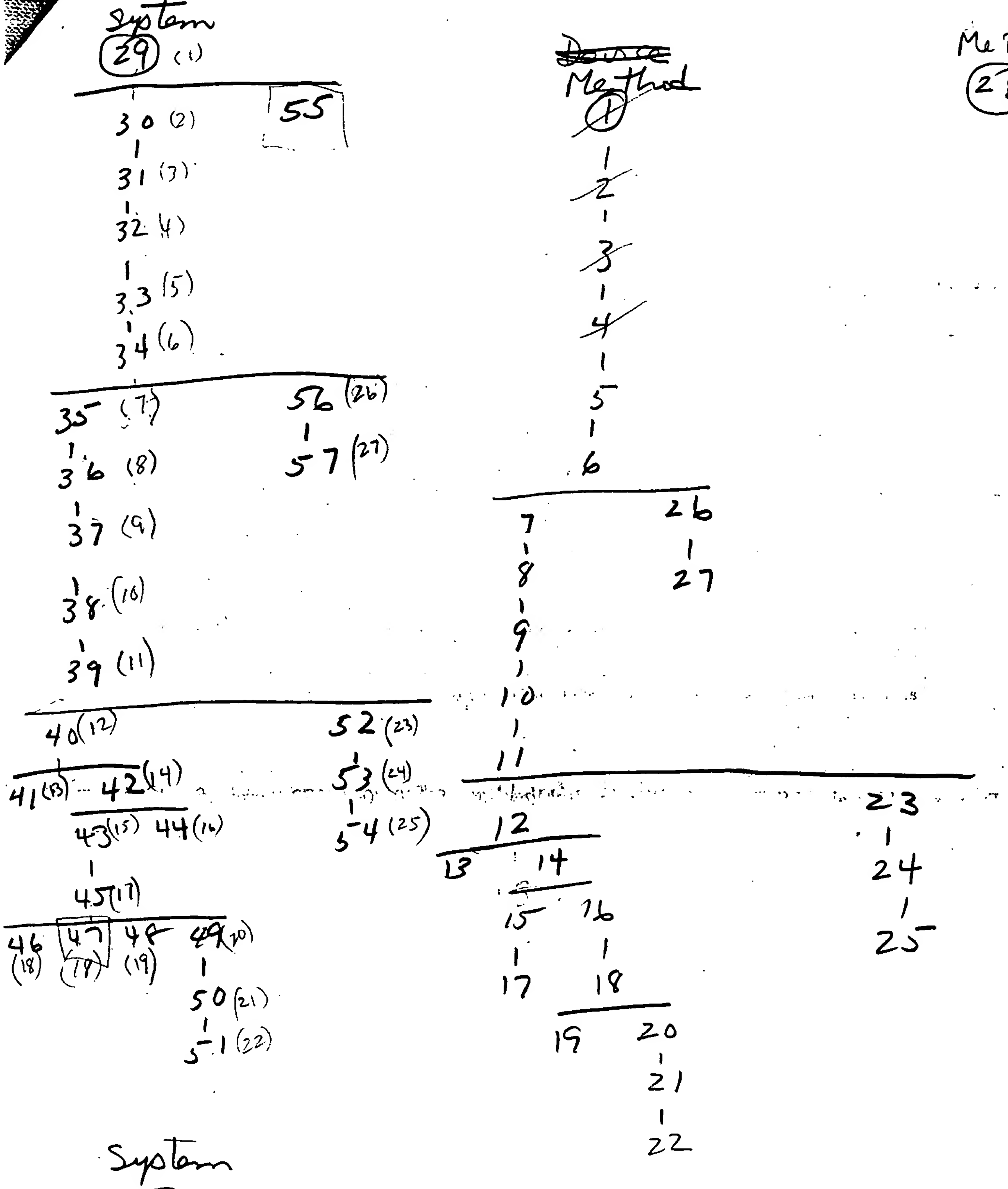

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